ABSTRACT OF THE DISCLOSURE

An amplifier circuit unit including a signal amplifying transistor is provided with a first bypass circuit unit for bypassing a part of an input signal to a ground side according to the strength of the input signal, and a second bypass circuit unit for bypassing a part of the input signal to an output side according to the strength of the input signal, whereby gain attenuation control is effected. Also, the amplifier circuit unit is provided with a control circuit unit for decreasing the a drain bias current of the signal amplifying transistor when the first bypass circuit unit bypasses the part of the input signal to the ground side, and interrupting the drain bias current of the signal amplifying transistor when the second bypass circuit unit bypasses the part of the input signal to the output side, whereby control of the drain bias current is effected.

and a choke coil Lb. The FET Q6 is cascade-connected with the signal amplifying FET Q1. Specifically, a source of the FET Q6 is connected to a drain of the signal amplifying FET Q1, and an output is extracted from a drain of the FET Q6.

The cascade-connected amplifier circuit can obtain a higher gain than a one-stage FET amplifier circuit. A gate of the FET Q6 is grounded via the bypass capacitance Cs3. The bias voltage VGG2 applied to the bias input terminal 40 is supplied to the gate of the FET Q6 as a gate bias voltage of the FET Q6 via the bias resistance Rg9.

Connected relations of the signal amplifying FET Q1, the bias resistance Rg1, and the choke coil Lb are the same as in the amplifier circuit unit 11 according to the first embodiment. As in the case of the second embodiment, the third embodiment is provided with the control circuit unit 34, and hence a source of the signal amplifying FET Q1 is grounded via a grounding capacitance Cs2 of the control circuit unit 34.

~~A~~ The fundamental configuration of the first bypass circuit unit 32, formed by a signal bypassing FET Q2, a bypass signal strength adjusting resistance Rc1, resistances Rg2 to Rg4, a coupling capacitance Cb1, and a

grounding capacitance Cs1, is the same as that of the first bypass circuit unit 12 according to the first embodiment. However, the signal bypassing FET Q2 is formed by M (M is an integer of 1 or more) FETs connected in series with each other.

Specifically, a drain of a FET Q21 in a first stage is connected to a gate of the signal amplifying FET Q1 via the coupling capacitance Cb1. A source of the FET Q21 is connected to a drain of a FET Q22 in a second stage. FETs in succeeding stages are connected in the same connected relation. Finally, a source of a FET Q2M - 1 in a (M - 1)th stage is connected to a drain of a FET Q2M in a final stage. The bypass control voltage CTL1 applied to the bypass control terminal 41 is supplied to gates of the FETs Q21 to Q2M in these stages via resistances Rg21 to Rg2M, respectively.

Connected relations of the other circuit components in the first bypass circuit unit 32, that is, the bypass signal strength adjusting resistance Rc1, the resistances Rg3 and Rg4, the coupling capacitance Cb1, and the grounding capacitance Cs1, are the same as in the first bypass circuit unit 12 according to the first embodiment.

~~A~~ The fundamental configuration of the second bypass circuit unit 33, formed by a signal bypassing FET

Q3, a bypass power adjusting resistance Rc2, resistances Rg5 and Rg6, and a coupling capacitance Cb2, is also the same as that of the second bypass circuit unit 13 according to the first embodiment. However, the signal bypassing FET Q3 is formed by N (N is an integer of 1 or more) FETs connected in series with each other.

Specifically, a drain of a FET Q31 in a first stage is connected to the gate of the signal amplifying FET Q1 via the coupling capacitance Cb1. A source of the FET Q31 is connected to a drain of a FET Q32 in a second stage. FETs in succeeding stages are connected in the same connected relation. Finally, a source of a FET Q3N - 1 in a (N - 1)th stage is connected to a drain of a FET Q3N in a final stage. The bypass control voltage CTL2 applied to the bypass control terminal 42 is supplied to the gates of the FETs Q31 to Q3N in these stages via resistances Rg51 to Rg5N, respectively.

Connected relations of the other circuit components in the second bypass circuit unit 33, that is, the bypass power adjusting resistance Rc2, the resistance Rg6, and the coupling capacitance Cb2, are the same as in the second bypass circuit unit 13 according to the first embodiment.

The thus formed, gain-controlled radio-frequency

amplifier circuit according to the third embodiment has the same configuration as the gain-controlled radio-frequency amplifier circuit according to the second embodiment, except that the plurality of signal bypassing FETs Q2 and Q3 are connected in series with each other. Therefore, the fundamental gain control operation of the gain-controlled radio-frequency amplifier circuit according to the third embodiment is the same as that of the gain-controlled radio-frequency amplifier circuit according to the second embodiment. However, the gain-controlled radio-frequency amplifier circuit according to the third embodiment is advantageous when applied ~~for~~to a higher-frequency band.

This is because, although ~~a~~the drain-to-source resistance when the FET is off may be assumed to be infinite, since ~~a~~ the drain-to-source capacitance Coff for a gate width of 400 μm in the case of a GaAs FET is about 0.1 pF, the one-stage signal bypassing FETs Q2 and Q3 cannot be ignored especially in higher-frequency applications, causing a decrease in the maximum gain when the FETs for bypassing to the ground side and the output side (Q2 and Q3) are cut off.

Thus, by the multiple-stage connection of the signal bypassing FETs Q2 and Q3, as in the gain-

controlled radio-frequency amplifier circuit according to the third embodiment, it is possible to reduce thea total drain-to-source capacitance Coff, and therefore, to avoid the adverse effects of a decrease in gain. Incidentally, an arbitrary number may be set as for each of the numbers M and N of stages for the multiple-stage connection of the signal bypassing FETs Q2 and Q3, and the numbers M and N of stages may be equal to each other (M = N). [Application]

The gain-controlled radio-frequency amplifier circuits according to the first to third embodiments described above are used to form a gain-controlled radio-frequency amplifier circuit (AGC amplifier) of an RF front end unit in a CDMA type portable telephone apparatus, for example. Fig. 4 is a block diagram showing an example of a configuration of an RF front end unit in a CDMA type portable telephone apparatus.

In Fig. 4, a received wave received by an antenna 41 is passed through a band allocation filter 42 used for both transmission and reception, changed to a certain signal level by an AGC amplifier 43, and then supplied to a mixer 44. The received wave is converted by the mixer 44 into an intermediate frequency (IF) by being mixed with a local oscillation frequency from a local